HIGH PERFORMANCE LOGIC AND HIGH DENSITY EMBEDDED DRAM WITH BORDERLESS CONTACT AND ANTISPACER

ABSTRACT OF THE DISCLOSURE

An integrated circuit such as a memory chip with embedded logic or a logic array or processor with imbedded large cache memory in which all significant sources of incompatibility between array transistors and high performance logic transistors are resolved. The integrated circuit includes memory cells having array transistors separated by minimum lithographic feature size, F, and memory cell areas or 8 - 12 F^2 and unsilicided metal bit lines encapsulated by a diffusion barrier while high performance logic transistors may be formed on the same chip without compromise of performance including an effective channel length of 0.7F or less, silicided contacts for low source/drain contact resistance, extension and halo implants for control of short channel effects and a dual work function semiconductor gate having a high impurity concentration and correspondingly thin depletion layer thickness commensurate with state of the art gate dielectric thickness. This structure is achieved by development of thick/tall structures of differing materials using a mask or anti-spacer, preferably of an easily planarized material, and using a similar mask planarized to the height of the structures of differing materials to decouple substrate and gate implantations in the logic transistors.